REMARKS

In the Official Action mailed on **14 December 2006**, the Examiner reviewed claims 1, 3-9, 11-17, and 19-27. Claims 1, 3-9, 11-17 and 19-27 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 1, 3-9, 11-17 and 19-27 were rejected under 35 U.S.C. §112, second paragraph as being indefinite. Claims 1, 3, 4, 6-9, 11, 12, 14-17, 19, 20, and 22-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Li et al (USPN 6,208,183, hereinafter "Li") in view of any one of Self et al. (USPN 6,112,308 hereinafter "Self '308"), (USPN 6,009,532 hereinafter "Self '532") in view of Bar-Niv (USPN 5,631,591 hereinafter "Bar-Niv"), in view of Oman et al. (USPN 4,635,186 hereinafter "Oman"), in view of Eggebrecht et al. (USPN 4,495,594 hereinafter "Eggebrecht), in view of Lenk (USPN 6,538,516 hereinafter "Lenk"), in view of Chesavage (USPN 6,239,626 hereinafter "Chesavage '626"), in view of Locker et al. (USPN 6,577,174 hereinafter "Locker"), in view of Doblar et al. (USPN 6,516,422 hereinafter "Doblar"), in view of Smith et al. (USPN 6,925,135 hereinafter "Smith"), in view of Yabuki et al. (USPN 5,332,978 hereinafter "Yabuki"). and further in view of Chesavage (USPN 6,925,135 hereinafter "Chesavage '350"). Claims 5, 13, and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Li et al. any one of Self '308, Self '532 in view of Bar-Niv, Oman, Eggebrecht, and further in view of any one Lenk, Chesavage '626, Locker et al., Doblar et al., Smith et al., Yabuki et al., Chesavage '350, and further in view of Coleman et al (USPN 4,151,473, hereinafter "Coleman").

Rejections under 35 U.S.C. §112

Claims 1, 3-9, 11-17 and 19-27 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Claims 1, 3-9, 11-17 and 19-27 were rejected under 35 U.S.C. §112, second paragraph as being indefinite.

Applicant has removed the language at issue in independent claims 1, 9, and 17. Applicant also respectfully points out that removing the language at issue makes the previous indefinite rejection moot.

Rejections under 35 U.S.C. §103(a)

Independent claims 1, 9, and 17 were rejected as being unpatentable over Li in view of any one of Self '308, Self '532, Bar-Niv, Oman, and Eggebrecht, and further in view of any one of Lenk, Chesavage '626, Locker, Doblar, Smith, Yabuki, Chesavage '350, and Coleman.

Applicant notes that it is difficult to settle two chips on a common frequency because of current leakages, parasitics, and/or nonlinearities. As a result, in some cases, each of the two chips may try to operate slightly more slowly than the other, and the control loop can consequently cause both chips' oscillators to slow down to a complete stop. This condition is addressed by the present invention (page 8, line 21 to page 10, line 2 and FIG. 2 of the instant application) by **introducing to the control loop a pair of edge detector circuits that gate two current sources, and an offset current source that is coupled to an integrating capacitor**. Using the small number of transistors shown, the modified control loop attempts to successively increase an oscillator's frequency to be just slightly higher than the other chip's frequency, until the slower chip's oscillator hits its maximum frequency. Once this point is achieved, the chip with a higher maximum frequency will continue to attempt to operate slightly faster than the maximum frequency of the slower chip, thereby ensuring that the combined circuits operate at a maximum shared frequency.

Applicant points out that **nothing in Li** in view of any one of Self '308, Self '532, Bar-Niv, Oman, and Eggebrecht, and further in view of any one of Lenk, Chesavage '626, Locker, Doblar, Smith, Yabuki, Chesavage '350, and Coleman **teaches a method for using edge detectors, gated current sources,**

and an offset current source to ensure that the chips' oscillators do not slow down due to current leakages, parasitics, and/or nonlinearities.

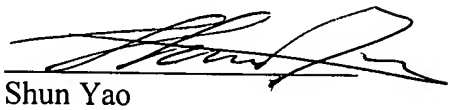
Accordingly, Applicant has amended independent claims 1, 9, and 17 to clarify that the present invention involves: 1) applying the internal frequency signal and the external frequency signals respectively to a first and a second edge detector circuit that are used to gate a first and a second (respective) current source; and, 2) using an integrating capacitor and an offset current source to ensure that the signal with a higher maximum frequency will operate at just above the maximum frequency of the signal with the lower maximum frequency. These amendments find support from page 8, line 21 to page 10, line 2 and FIG. 2 of the instant application. Dependent claims 2, 10, and 18 have been canceled without due prejudice. No new matter has been added.

Hence, Applicant respectfully submits that independent claims 1, 9, and 17, as presently amended are in condition for allowance. Applicant also submits that claims 3-8 and 25, which depend upon claim 1, claims 11-16 and 26, which depend upon claim 9, and claims 19-24 and 27, which depend upon claim 17, are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

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